Performance Analysis of Multi-radio Transmitter with Polar or Cartesian Architectures associated with High Efficiency Switched-Mode Power Amplifiers.

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Invited paper

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Abstract. *This paper deals with wireless multi-radio transmitter architectures operating in the frequency band of 800 MHz – 6 GHz. As a consequence of the constant evolution in the communication systems, mobile transmitters must be able to operate at different frequency bands and modes according to existing standards specifications. The concept of a unique multiradio architecture is an evolution of the multistandard transceiver characterized by a parallelization of circuits for each standard. Multi-radio concept optimizes surface and power consumption.*

Transmitter architectures using sampling techniques and baseband ΣΔ or PWM coding of signals before their amplification appear as good candidates for multiradio transmitters for several reasons. They allow using high efficiency power amplifiers such as switched-mode PAs. They are highly flexible and easy to integrate because of their digital nature. But when the transmitter efficiency is considered, many elements have to be taken into account: signal coding efficiency, PA efficiency, RF filter. This paper investigates the interest of these architectures for a multiradio transmitter able to support existing wireless communications standards between 800 MHz and 6 GHz. It evaluates and compares the different possible architectures for WiMAX and LTE standards in terms of signal quality and transmitter power efficiency.

Keywords

Multiradio transmitter, high-efficiency RF transmitter, polar transmitter architectures, Cartesian transmitter architectures, class E power amplifier, ΣΔ coding, PWM coding, WiMAX, LTE.

1. Introduction and Context

Wireless communications systems including cellular communications, personal area networks (PANs), local area networks (LANs) and metropolitan area networks (MAN) have presented a considerable development in recent years and keep evolving constantly. Coexistence of different wireless standards on a same device is necessary to satisfy the users who expect mobility, ubiquitous connection and high data rates at the same time. This coexistence should not increase the size of the device or reduce its battery life. The goal of this evolution is to reduce the number of external components and to increase the integration in the low-cost CMOS technology. Another stage which pursues the evolution towards the cognitive radio and implies flexibility of each stage of the communication chain is the cognitive Multi-Radio. Instead of including an independent architecture for each standard, universal transmitter architecture capable of generating all the different standards waveforms seems to be the best solution (especially in terms of consumed power and surface occupation). This concept is known as multi-radio transmitter. Cognitive Multi-Radio has the capability of the multistandard concept and moreover it is capable to perform an efficient environment spectrum scanning and react to the environment conditions choosing the appropriated communication standard. At present, we envisage a cognitive multi-radio able to support existing wireless communications standards between 900 MHz and 6 GHz. Principal parameters to consider in a multi-radio signal for each standard are bandwidth, power dynamic range and envelope magnitude range (expressed by the Peak to Average Power Ratio – PAPR) which depend on the modulation type. From the mobile multi–radio transmitter point of view, key aspects to consider are power efficiency and linearity. Moreover, transmitted signal is limited to the frequency band assigned by local regulation and must respect established limits of adjacent channel power ratio (ACPR) and power spectrum emission mask. If required, transmitter must be able to adjust its output power over a defined range. Multi-radio architecture should handle variations of previously enounced parameters respecting all standards requirements.

To overcome the implementation design complexity, linearization methods or highly linear non-constant envelope architectures able to transmit high PAPR signals must be investigated. In this context, different constant envelope

architectures (CEAS) have been proposed. In these architectures, the input of the power amplifier (PA) is a constant envelope signal even if the useful signals at the input and output of the transmitter have a time varying envelope. The potential interest of such architectures is to allow the use of high efficiency power amplifiers such as switched-mode PAs. But in order to regenerate the original varying envelope signal, an RF filter is most of the time necessary at the output of the PA. Therefore when efficiency is considered, many elements have to be taken into account: signal coding efficiency, PA efficiency, RF filter.

Among the CEAS transmitter architectures, we can distinguish at least 3 kinds of approaches. In the first one, the signal envelope (i.e. its magnitude) is used to modulate in amplitude the PA power supply such as EER (envelope elimination and restoration) [1], [2], envelope tracking [3], [2] and the different kinds of dynamic power supply techniques [2] or polar lite architectures [4]. In the second one such as LINC (Linear amplification with non-linear component) [5] or CALLUM (Constant Amplitude Locked Loop Universal Modulator) [6], the original signal with time varying envelope is decomposed in a sum of 2 constant envelope signals that are amplified by two identical PA and recombined at the output of PAs. In the third one, the time varying original signal is sampled and coded into a 2-level signal [7] to generate a constant envelope signal. These different approaches can be combined such as in EER-LINC architectures [8].

In this paper, we focus on RF Transmitters with switched-mode PA and CEAS architectures using sampling techniques and baseband ΣΔ or PWM coding of signals and we analyze their interest for multiradio transmitters. In section 2, we present the principles of polar and cartesian sampled CEAS architectures with baseband ΣΔ or PWM coding. In section 3, we describe the results obtained by simulation for the different architectures and compare the different approaches from the point of view of signal quality and power efficiency. This section is split in 2 parts: the first one analysis the quality of the reconstructed signal in the case of an ideal PA and the second one presents the results with a switched class E PA.

2. Principles of Constant Envelope Architectures using Sampling Techniques

In the following, we will call "original signal" the signal at the input of the transmitter that has potentially a time varying envelope. CEAS architectures using sampling technique (that we will note CEAS) rely on the coding of the original signal into a constant-envelope signal that is usually a two-level signal from which the original signal can be restored by a filtering operation. We will call this signal the "coded signal". The coding operation is sometimes called modulation. The most frequent coding techniques are PWM (Pulse Width Modulation) and ΣΔ modulation (or coding). These coding techniques take profit of an oversampling operation before the two-level coding.

Historically, the first CEAS architecture using sampling techniques is the LIST architecture (Linear amplification using sampling technique) that was proposed by Cox [7]. The LIST architecture is described in Fig. 1.

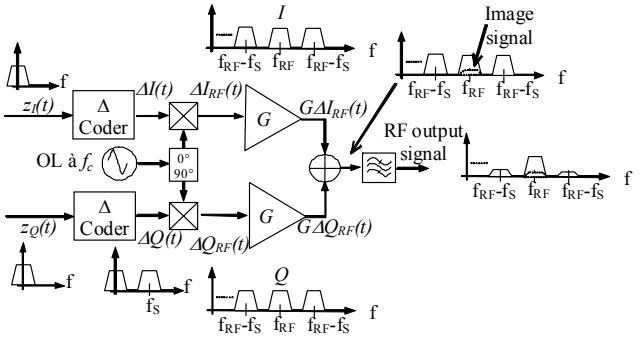

Fig. 1. LIST architecture proposed by Cox [7].

The real and imaginary parts of the complex envelope of the original signal are oversampled and coded by delta coders. These two coded signals modulate in amplitude two carriers in quadrature. The resulting frequency transposed signals have a constant envelope. They are amplified by two high efficiency PAs whose output are summed. Finally, the signal is filtered by a pass-band filter to regenerate the amplified original signal. One of the critical point of the LIST architecture is the efficient combining of the outputs of the two PAs.

The signal to noise ratio (SNR) after the signal reconstruction depends on the oversampling ratio. Typically with the LIST approach, for an SNR of 55 dB, it should be greater than 200*B* where *B* is the signal bandwidth.

A general question for CEAS architectures is the bandwidth *B* of the output RF bandpass filter signal to consider. In a multi-channel system, the bandwidth *B* should be the total bandwidth of the system and not the bandwidth of a single channel. This allows using the same RF bandpass filter whatever the channel but of course it increases the necessary oversampling frequency.

New CEAS architectures have been proposed in the literature using PWM or ΣΔ modulation. We can distinguish two approaches, depending on whether the RF or the baseband signals are coded.

Fig. 2 illustrates the case where the RF signal is coded [9]. In this architecture the RF modulated signal is directly coded by a bandpass ΣΔ [10] or PWM modulator. This approach is based on a 1 bit quantization of the RF modulated signal. Resulting constant envelope signal drives a Switched mode PA followed by a band-pass filter in order to reduce ΣΔ noise. The main difficulty of this approach is the necessary sampling frequency that is typically equal to 4 times the carrier frequency for the bandpass ΣΔ modulator. In the case of high frequency carrier (typi-

cally above 2 GHz) it is still very difficult or impossible to realize coders at such high frequencies.

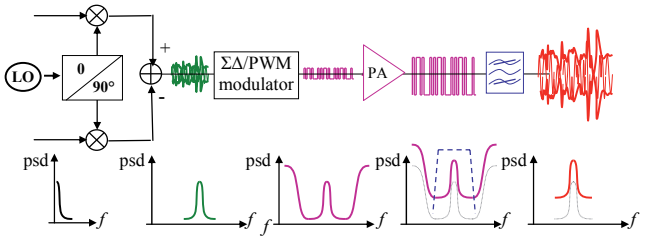

Fig. 2. Principle of CEAS architecture with coding of the RF signal showing the spectrum shapes (psd power spectral density) of signals.

There are several possible baseband approaches depending on how the complex envelope is processed. They differ in particular on whether cartesian or polar coordinates are processed and on whether PWM or ΣΔ coders are used. We can therefore distinguish: polar ΣΔ, Cartesian ΣΔ, polar PWM and Cartesian PWM architectures. And for each of these architectures, different electronic implementations can be proposed. In the following, we will note $z(t)$ the complex envelope, $z_I(t)$, $z_Q(t)$ its Cartesian coordinates and $\rho(t)$, $\varphi(t)$ its polar coordinates, with the following relation:

$$z(t) = z_I(t) + jz_Q(t) = \rho(t)\exp\left(j\varphi(t)\right). \tag{1}$$

2.1 Principles of Polar ΣΔ or PWM CEAS Architectures

Two approaches have been originally proposed for polar ΣΔ or PWM CEAS transmitters [11], [12]. In this paper we focus on the first one, which uses a "±a 1-bit ΣΔ or PWM coder" (2 opposite level output). It is presented in Fig. 3 extracted from [11]. In the figures of this section, we represent a 1-bit ΣΔ coder but it can be replaced by a PWM coder.

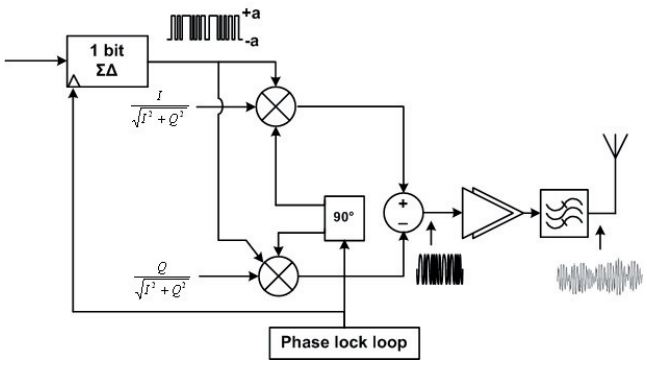

Fig. 3. Polar CEAS architecture.

In this architecture, envelope and phase restoration is carried out in baseband before the power amplifier.

In a polar CEAS architecture, data are mapped following a given modulation to generate the complex envelope $z(t)$. The resulting complex envelope is decomposed in its polar coordinates and the baseband envelope and phase signals $\rho(t)$, $\cos(\varphi(t))$, $\sin(\varphi(t))$ are constructed. Then, the envelope signal $\rho(t)$ is coded by a low-pass ΣΔ or PWM modulator and the output of the 1–bit coder is a two-level constant envelope signal noted $\rho_{coded}(t)$ with $\rho_{coded}(t) = \pm a$. We will call coded envelope, the signal $\rho_{coded}(t)$. Phase signal $\exp(j\varphi(t))$ and coded envelope are recombined to form a constant envelope signal $\rho_{coded}(t)\exp(j\varphi(t))$. This signal is frequency up-converted with at the carrier frequency f_c (with $\omega_c = 2\pi f_c$ to form the RF modulated signal $x(t)$:

$$\begin{aligned} x(t) &= \Re\left(\rho_{coded}(t)\exp\left(j\varphi(t)\right)\exp\left(j\omega_c t\right)\right), \\ &= \rho_{coded}(t)\left(\cos\left(\varphi(t)\right)\cos\left(\omega_c t\right) - \sin\left(\varphi(t)\right)\sin\left(\omega_c t\right)\right), \\ &= \rho_{\Sigma\Delta}(t)\cos\left(\omega_c t + \varphi(t)\right). \end{aligned} \tag{2}$$

The RF modulated signal $x(t)$ is sent to the power amplification. As $x(t)$ is a constant envelope signal, linearity requirements are relaxed for the PA and a switched mode PA can be used. Delay mismatch is not as severe issue as in the classical EER [13] architecture. Amplified signal is finally filtered.

To keep ΣΔ modulator stability, an input level controller must be included at the input of the ΣΔ modulator.

Different electronic implementation can be applied for this architecture. We can generate the two signals $\rho_{coded}(t)\cos(\varphi(t))$ and $\rho_{coded}(t)\sin(\varphi(t))$ in a digital way. Therefore, two digital-to-analog converters are necessary before the RF IQ modulator as depicted in Fig. 4. DACs sampling frequency is chosen according to the ΣΔ or PWM frequency. It has to be high enough to avoid ΣΔ or PWM noise overlapping. Targeted communication standards in new cellular systems and wireless local area network require high ΣΔ or PWM frequencies and therefore significant sampling frequency for DACs.

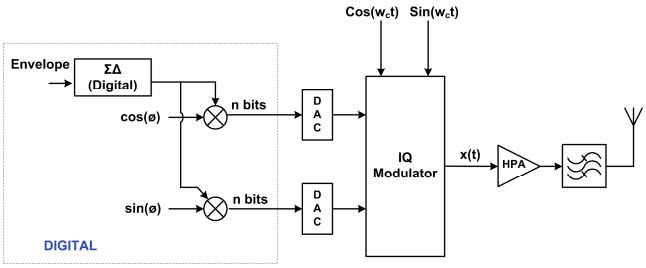

Fig. 4. Polar CEAS architecture with digital I and Q signals.

A second possible implementation of the architecture is presented in Fig. 5. The output of the low-pass ΣΔ or PWM modulator is analog. The digital phase (or instantaneous frequency) signal is converted to analog and then modulated to the carrier frequency with a modulated PLL. Finally constant envelope and phase signals are recombined.

The advantage of this approach compared to the first one is that it requires only one DAC. Furthermore, DAC frequency requirements are mitigated. But the bandwidth

of the phase signal can be a challenge for the modulated PLL. In that case, the modulated PLL can be replaced by an IQ modulator but two DAC are necessary to generate $\cos(\varphi(t))$ and $\sin(\varphi(t))$.

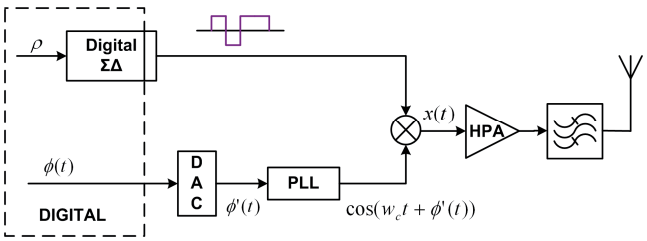

Fig. 5. Polar ΣΔ architecture with modulated PLL.

In the first architecture, modulation to the carrier frequency is performed by the IQ modulator block with help of an analog mixer. Similarly, the second architecture makes use of an analog multiplier to recombine envelope and phase.

A third possible architecture (see Fig. 6) proposes to generate a digital carrier and then to replace the analog mixer by a digital one, like an AND gate for example. We will refer in that case to digital mixed signal.

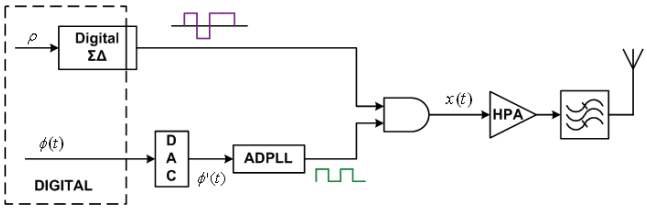

Fig. 6. Polar ΣΔ architecture with digital mixing.

We consider that digital mixing is advantageous for polar sigma delta architecture, not only it offers all the typical advantages of a digital signal treatment but it also offers IC integration.

Synchronization between envelope and phase signals is a critical aspect in polar architectures. To overcome this problem, it is suggested in this third approach to use the same frequency generator for the ADPLL reference and for the ΣΔ or PWM modulator. This is a practical implementation because only one frequency generator is needed in the architecture.

Some studies on a fully digital implementation based on a radio-frequency DAC are presented in [14].

2.2 Principles of Cartesian ΣΔ or PWM CEAS Architectures

Instead of using polar coordinates, we have proposed to separate base-band modulated signal into its In-Phase and Quadrature components leading to a "Cartesian" CEAS transmitter architecture [15].

In the proposed Cartesian ΣΔ or PWM transmitter CEAS architecture data are mapped and treated in base-band according to the chosen modulation requirements. Resulting signal is separated in its In-Phase (I) and Quadrature (Q) components. I and Q components are non constant envelope signals, so two 1-bit lowpass ΣΔ or PWM modulators are used to code and transform them in signals varying between +/- a. Resulting I and Q coded signals have constant envelope, they are RF modulated and recombined before power amplification. The PA input is then a constant envelope signal. Finally, amplified signal is filtered by a bandpass filter centered at the carrier frequency (Fig. 8).

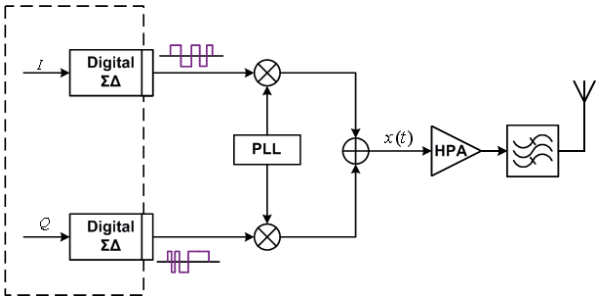

Fig. 8. Cartesian ΣΔ transmitter architecture.

3. Simulation and Comparison of CEAS Polar and Cartesian Architectures

The polar and cartesian CEAS architectures have been simulated and compared with WiMAX and LTE input signals. Simulations and comparisons have been done first with an ideal PA to evaluate the influence of the sampling frequency on the quality of the reconstructed signal and secondly with a class E switched-mode PA to evaluate the efficiency of the full transmitter. All the simulations were conducted using the Agilent Advanced Design Software (ADS).

3.1 Input Signals Used for the Tests

Mobile WiMAX and LTE standards have been adopted for simulations because they support a very demanding modulation in terms of envelope PAPR and bandwidth.

According to the WiMAX forum implementation profiles, four primitive parameters characterize the OFDMA symbol: channel bandwidth (BW), number of used subcarriers including data and DC subcarriers (N_{used}), sampling factor (n) and cyclic prefix to useful time ratio (G) [16]. One of the implementation profiles proposed by the WiMAX Forum was selected for mobile WiMAX simulations: a 10 MHz channel - 1024 FFT size, "n" factor and cyclic prefix to useful time ratio G were fixed to 57/50 and 1/32 respectively. A 64-QAM modulation is considered in simulations to achieve the highest PAPR signal. Obtained symbol rate is 11 Msymb/s.

WiMAX standard defines a power spectral mask for unlicensed bands (10 and 20 MHz channels), even if mobile WiMAX only can be deployed in licensed bands, this mask can be taken as a reference: for the 10 MHz channel -50dBc must be reached at 14.5 MHz from carrier. Furthermore, ETSI has defined masks for the channel bandwidths that were originally proposed in 802.16d. Adapting the ETSI mask for the 10 MHz channel, -50dBc must be reached at 20 MHz from carrier. We have considered one of the frequency bands proposed by the WiMAX Forum for mobile WiMAX with a bandwidth of 100 MHz.

LTE is a multi-carrier standard specified by the 3GPP consortium. It is an evolution of the cellular phone standards that targets high data rates, up to 70 Mbps in uplink and up to 300 Mbps in downlink for a 20 MHz channel and a 4x4 MIMO configuration. LTE disposes of the same frequency bands as those allocated to UMTS [17]. It uses OFDMA (Orthogonal Frequency Division Multiple Access) in the downlink direction, while the uplink is based on SC-FDMA (Single Carrier Frequency Division Multiple Access). LTE output power limits may vary depending on the frequency band, nevertheless maximal value is 23 dBm. The minimum requirements for the Error Vector Magnitude (EVM) are 17.5% for QPSK, 12.5% for 16-QAM and 8% for 64-QAM [17].

For the simulations, we used Uplink SC-FDMA signals generated using the LTE source provided by the ADS software. The 1920 – 1980 MHz frequency band (E-UTRA Band number 1) has been chosen for this study. A 10 MHz channel bandwidth has been selected; it defines 50 resource blocks, 600 useful data sub-carriers and an FFT size of 1024. Each sub-carrier is modulated by QPSK. Normal cyclic prefix is used for symbol generation and hence there are 6 symbols per slot. The total bandwidth of LTE is 60 MHz.

3.2 Antenna Filter

Antenna filter should guarantee minimal ripple over the targeted bandwidth and also present enough stopband attenuation in order to respect power emission mask. Ripple of 1 dB and out of band attenuation of 51 dB were fixed for the filter conception. Elliptic type filter was considered because its transfer function is quite similar to that of Bulk Acoustic Wave (BAW) filters [18]. BAW filters are designed associating Film Bulk Acoustic Resonators (FBARs). We envisage BAW filters as good candidates for Multiradio applications because they handle high power levels and offer significant band rejection and high operation frequency. Moreover, they can be integrated "above IC", which means size reduction and package simplicity [18].

3.3 Characteristics of the ΣΔ Modulator

Envelope ΣΔ modulators used in the polar and the Cartesian architectures have the same transfer function. This ΣΔ modulator has been synthesized using the Matlab Delta-Sigma Toolbox [19]. The choice of the sampling frequency $f_{\Sigma\Delta}$ is a critical point. Choosing a high $f_{\Sigma\Delta}$ improves the signal to noise ratio (SNR) for the reconstructed signal but increases the power consumption of the ΣΔ coder. It can be shown that to minimize ΣΔ noise folding and to improve the SNR, $f_{\Sigma\Delta}$ must verify the following conditions, where f_c is the carrier frequency and m an integer:

$$\begin{cases} f_{\Sigma\Delta} < 2f_c, \\ f_{\Sigma\Delta} = \dfrac{2f_c}{m}. \end{cases} \tag{3}$$

For the WiMAX and LTE cases of the simulations, we have chosen $f_{\Sigma\Delta} = f_c$ which give the best possible oversampling ratio (OSR). For the simulation we have chosen f_c =3.7 GHz for WiMAX and f_c = 1.96 GHz for LTE. The OSR is equal to 18 for WiMAX and to 16 for LTE.

With these input parameters, the noise transfer function (NTF) obtained with the "synthetizeNTF" toolbox function is:

$$NTF = \frac{(z-1)^2}{z^2 - 0.8396z + 0.2657}.$$

A feedback ΣΔ structure (Fig. 9) has been selected instead of a feedforward structure because of its response flatness, less overvoltage risk and better stability. Using the "realizeNTF" function a, b, c, and g coefficients are obtained.

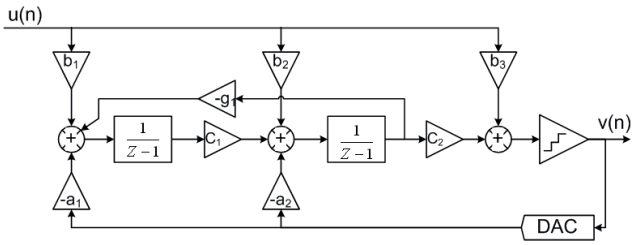

Fig. 9. Cartesian ΣΔ transmitter architecture.

3.4 Characteristics if the PWM Modulator

In the different CEAS architectures, a PWM modulator can be used instead of a ΣΔ modulator. There are different ways to realize a PWM modulator. In analog PWM modulators, a periodic reference signal with a frequency (f_{pwm}) is compared with the input signal and the 2-level value of the coded output depends on the result of the comparison. Different reference signals can be used such as symmetrical triangular or sawtooth signals. The original input signal is regenerated by applying a low-pass filter to the PWM modulator output. The SNR between the original and regenerated signals depends on the frequency of the reference signal. Typically, PWM modulator frequency (f_{pwm}) is not as elevated as the ΣΔ modulator frequency. For simulations purposes and aiming to compare results with both architectures, f_{pwm} has been

chosen to be a sub-multiple of the ΣΔ sampling frequency $f_{\Sigma\Delta}$. We have chosen: $f_{pwm} = f_{\Sigma\Delta}/10$. It is therefore equal to 370 MHz for the WiMAX case and to 196.6 MHz for the LTE case. A sawtooth reference signal has been used. PWM minimum time (T_{pwm}) has been initially fixed to be the same as the ΣΔ output minimum time ($T_{\sigma\delta}$). The PWM modulator output signal varies between [-A, A].

3.5 Simulation Results and Comparison with an Ideal Power Amplifier

The results of this section are obtained with an ideal PA.

Simulation results for the Cartesian ΣΔ architecture: Fig. 10 shows the power spectral densities (psd) of the signals before and after the RF filter for the Cartesian ΣΔ architecture.

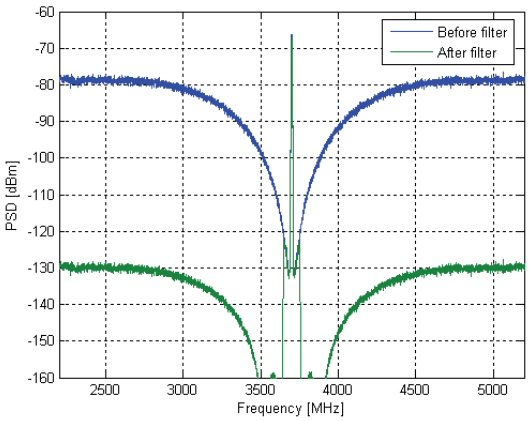

Fig. 10. Signal psd before and after the RF band-pass filter for the Cartesian architecture.

Power mask is respected as it can be verified in Fig. 11 which is a zoom of Fig. 10 around the carrier frequency.

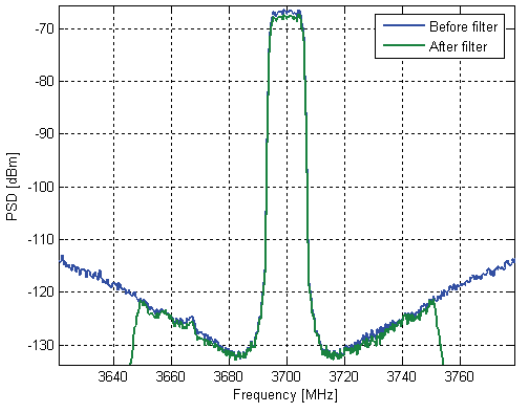

Fig. 11. Transmitted signal spectrum (zoom).

In order to estimate EVM transmitter contribution, an ideal receiver was simulated. EVM is found to be 0.38%.

Simulation results for the Polar ΣΔ architecture: This section presents the results obtained with a Polar ΣΔ transmitter architecture as described by Fig. 3. Simulation parameters are the same as those used for the Cartesian ΣΔ architecture simulation.

Envelope bandwidth is higher than I and Q signals bandwidth (about 30 MHz instead of 5 MHz). Fig. 12 shows transmitter output spectrum before and after filtering (using the same filter as for the Cartesian architecture). Transmitted signal also respects the power mask and EVM is found to be 0.46%.

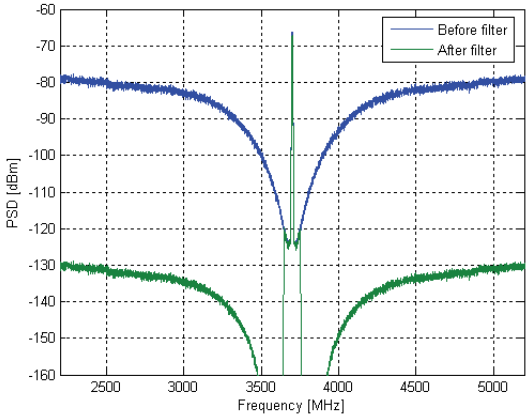

Fig. 12. Signal spectrum before and after the band-pass filter for the polar architecture.

Comparison of the Cartesian and the Polar ΣΔ architectures: In conclusion, the polar and Cartesian architectures give similar results from the point of view of signal quality (spectrum and EVM) but the Cartesian architecture is slightly easier to implement.

One advantage of the Cartesian architecture in comparison to the polar architecture is that for the same sampling frequency, OSR can be higher because I and Q signals bandwidth is narrower than envelope bandwidth.

Furthermore, in polar ΣΔ architecture a Digital to Analog Converter (DAC) is necessary for the phase signal (an ideal one was considered in the simulation). Cartesian architecture doesn't need this extra component because conversion is directly performed by the ΣΔ modulators (I and Q signals). Besides, a digital mixing architecture as proposed before with a digital carrier and a digital mixer (like an AND gate for example) instead of an analog one, can be directly implemented with the Cartesian architecture. Finally, because I and Q paths in the Cartesian architecture are symmetrical, the Cartesian ΣΔ architecture is less sensible to mismatching effects than the Polar one.

The results of this comparison are valid only for an ideal PA and do not take into account efficiency aspects that are considered in the next section. In particular it is interesting to analyze the influence of the envelope coding on the PA efficiency in the case of a switched mode PA.

3.6 Comparison of the Architectures with a Switched-Mode PA

In order to characterize the architecture with a switched-mode PA, we have designed an amplifier operating in class E. First, we recall the advantages and principles of switched mode amplifiers.

Switched-mode PA:

Switched-mode power amplifier (Sw PA) topology has been chosen for efficiency improvement [10]. There are different classes of Sw PAs (D, S, E and F), based on different transistor behavior and reactive elements of the load network. Class D and S are used in pulsed and low-pass applications like audio, and do not provide a bandpass filtering of the signal as needed in wireless communications. Class E and F are suitable for RF applications [2], [20]. Class F PA is based on several resonating networks with high Q factors which are difficult to implement. Class E PA uses an inductor and a shunt capacitor to balance the parasitic output capacitance of the transistor. The topology used to design the amplifier is described below (Fig. 13) and is named "serial inductor".

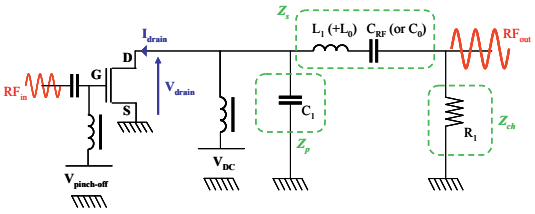

Fig. 13. Serial inductor topology of a Class E amplifier.

A high efficiency PA is based on maximum voltage at zero current and vice versa, without any DC power dissipation. From this theoretical hypothesis, it is possible to calculate the optimum value of Class E output network element. In this case, the output of the transistor is supposed to be a short or an open circuit and the quality factor (Q) of C_0-L_0 is considered as infinite (perfect filtering conditions). In the signal provided by the architecture, information appears around the fundamental frequency and most of the power is spread over a wide spectrum including the two first lobes. A finite value of Q ($Q = 8$) guarantees good switching conditions. The load has been set to 50 Ω (R_1) considering emission filter and antennas as ideal. The calculation for Class E network components is:

$$C_0 = \frac{1}{(Q - 1.15249) \times Rload \times \omega_0}, \; L_0 = \frac{1}{C_0 \omega_0^2}, \quad (4)$$

$$C_{shunt} = \frac{0.1836}{Rload \times \omega_0} - C_{DS}, \quad (5)$$

$$L_{serial} = \frac{Rload \times 1.15249}{\omega_0}. \quad (6)$$

In this study we use a GaAs E-PHEMT, Avago ATF50189 transistor.

It is a high linearity and medium power FET (29dBm output power at 1dB gain compression). The class E amplifier has been designed to work at LTE frequency band. Input matching network has been designed keeping in mind that it should not filter the wide spectrum signal provided by the architecture. The goal is to preserve constant envelope property while mainly amplifying the information. Simulated amplifier performances show drain efficiency (η_D) of 92%, overall efficiency (η_0) of 89% and 14dB of gain for 5 dBm 1-tone input signal.

From the amplifier results, it is possible to analyze the performances of each architecture.

The performances are evaluated by the EVM and the efficiency. For the EVM, Tab. 1 gives the value in the case of a WiMAX signal characterized by a channel bandwidth of 10 MHz, 64 QAM modulation, and sampling frequency equal to three times of carrier frequency [21].

	PWM	Polar ΣΔ	Cartesian ΣΔ
EVM	5,1%	1.4%	3.3%

Tab. 1. EVM value for the WiMAX case with a class E PA.

It may be noted that the EVM values in the case of LTE signal are of the same order.

We evaluated the efficiencies in the case of the LTE signal in Tab. 2.

Parameters	PWM	Polar ΣΔ	Cartesian ΣΔ
Pin	6 dBm	6 dBm	6 dBm
Pout	16,6 dBm	13,9 dBm	12 dBm
Drain Efficiency	79,2 %	61 %	34,8 %
PAE	72,3 %	51,1 %	26,1 %
Global Efficiency	74 %	55,5 %	32 %
Global Gain	10,6 dB	7,9 dB	6 dB
PAE_BW (60 MHz)	22,2 %	30,2 %	4,6 %

Tab.2. Efficiency results for the LTE case with a class E PA.

4. Conclusion

This paper concentrates on flexible multi-radio architectures. This kind of architectures could be used in the future for cognitive radio applications. Three architectures have been analyzed and compared: the polar architecture with ΣΔ envelope modulator, the polar architecture with pulse width modulator and the cartesian ΣΔ architecture. Validation is accomplished with the most critical signals in terms of power dynamics and frequency bandwidth; these are the LTE and mobile WiMAX.

PWM architecture shows better power efficiency. But, it was shown that although the global efficiency of ΣΔ polar architecture was lower than PWM architecture, performance in the band of interest around the carrier was better. The polar ΣΔ architecture provides an output power lower than the PWM architecture but slightly degrades the emitted signal. Cartesian ΣΔ architecture is that which has the lowest output power and efficiency. The final choice of architecture is a compromise between required perform-

ances and reconfigurability. Moreover, taking into account the emission filter in an integrated technology involves a co-design.

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